DETAILED ACTION

The examiner acknowledges the applicant's submission of an amendment dated 7/11/2008. At this point claims 1 and 7 have been amended. Claims 15 and 18 have been cancelled. Thus, claims 1-14, 16, 17, 19 and 20 are pending in the instant application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 7, 11, 13, 17 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1, 7, 11, 13, 17 and 20 recite, "each non-contiguous physical memory address space corresponds to a different memory device of the multiple memory devices". However, nowhere in the specification discloses that each flash memory devices includes a non-contiguous address sub-range. Upon expecting the specification, especially paragraph 35, the examiner concludes that the sub-ranges are non-contiguous because they are materialized in a plurality of different memory devices,

not because each of the plurality of memory devices contains a non-contiguous address range within itself.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-14, 16, 17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen et al. (US 5,067,105) in view of Daberko (US 5,787,445).

2. As per **independent claims 1, 7, 11, 13, 17 and 20**, Borkenhagen et al. discloses, "receiving a command comprising a first logical memory address **[Receiving a logical card memory address, Column 3, Lines 60-64]** from the range of logical memory addresses **[Logical Memory addresses, Column 3, Lines 60-64]**".

"accessing a look-up table having logical memory addresses with their corresponding physical memory addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of the plurality of physical memory address to find a first physical memory address, from a range of physical memory addresses, that corresponds to the first logical memory address **[Determining a**

physical card memory address that corresponds to the logical card memory address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]"

"Generating a chip select signal to one of the plurality of the multiple memory devices in response to the first physical memory address **[Selecting a physical card based on the physical card memory address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]** wherein the plurality of ranges of physical memory addresses include non-contiguous physical memory address space such that each non-contiguous physical memory address space corresponds to a different memory device of the multiple memory devices **[independent physical storage cards, Figure 2]**".

Borkenhagen et al. do not disclose expressly, "the single flash memory device having the contiguous range of logical memory addresses".

Daberko discloses, "flash RAM" in column 3, at lines 14-16.

Borkenhagen et al. and Daberko are analogous art because they are from the same filed of endeavor of increasing fault tolerance by memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Borkenhagen et al. by including a "flash RAM" as taught by Daberko in column 3, at lines 14-16.

The motivation for doing so would have been increased fault tolerance to power interruption as expressly taught by Daberko in column 3, at lines 23-25.

Therefore, it would have been obvious to combine Daberko with Borkenhagen et al. for the benefit of increased fault tolerance to obtain the invention as specified in claims 1, 7, 11, 13, 17 and 20.

3. **Claim 2** discloses, "the range of physical memory addresses is contiguous **["physical memory addresses" sharing the same "physical card memory address", (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**".

4. **Claim 3** discloses, "the range of physical memory addresses is substantially equivalent to the range of logical memory addresses **[The "logical memory address" and the corresponding "physical memory address" are identical except the first 3-bits (The identical memory addresses are materialized in a different physical memory card), (Column 3, Line 60 – Column 4, Line 10)]**".

5. **Claim 5** discloses, "the range of logical memory addresses are contiguous and the corresponding range of physical memory addresses is non-contiguous and comprised of a plurality of physical sub-ranges **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**".

6. **Claim 6** discloses, "a chip select signal **[Selecting a physical card based on the physical card memory address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]** is generated for each physical memory address sub-range **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**".

7. **Claim 7** discloses, "receiving a command comprising a first logical memory address **[Receiving a logical card memory address, Column 3, Lines 60-64]** from the range of logical memory addresses **[Logical Memory addresses, Column 3, Lines 60-64]**".

"accessing a look-up table having logical memory addresses with their corresponding physical memory addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of ranges of physical memory addresses to find a first physical memory address, from a range of non-contiguous physical memory addresses **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**, that corresponds to the first logical memory address **[Determining a physical card memory address that corresponds to the logical card memory address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]**"

"Generating a chip select signal in response to the first physical memory address **[Selecting a physical card based on the physical card memory address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**"

8. **Claim 8** discloses, "a controller circuit executing an application in which the first logical memory address is read from memory **[CPU executing an application and generating a logical memory address, Figure 1, Column 3, Lines 60-68]** along with the command".

9. **Claim 9** discloses, "a device manager receiving the first logical memory address **[Physical card selector logic receiving the first logical memory address, Figure 1]** from a controller circuit".

10. **Claim 10** discloses, "the device manager generates the chip select signal **[Physical card selector logic selecting appropriate chip, Figure 1, (Column 3, Line 65 – Column 4, Line 10)]** in response to the first physical memory address".

11. As per **claim 4**, **Daberko discloses, "flash RAM" in column 3, at lines 14-16.**

12. **Claim 12** discloses, "the plurality of non-contiguous sub-ranges is substantially equal to a logical memory address range of a flash memory device **[The "logical memory address" and the corresponding "physical memory address" are**

identical except the first 3-bits (The identical memory addresses are materialized in a different physical memory card), (Column 3, Line 60 – Column 4, Line 10)]".

13. **Claim 14** discloses, "the controller circuit is coupled to the plurality of flash memory through a plurality of memory address lines **[Figure 3C, Daberko]**".

14. **Claims 16 and 19** disclose, "the controller circuit generates the first physical memory address in response to adding a memory address offset to the first logical memory address **[the difference between the generated physical memory address and the logical memory address is the "offset", Figure 1]**".

Arguments Concerning 35 USC 112 Rejections

Regarding claims 1, 7, 11, 13, 17 and 20, the applicant argues that the specification defines the claim limitations of "each of the plurality of non-contiguous sub-ranges corresponding to a different one of the plurality of flash memory devices". However, the examiner maintains his position regarding the issue because the applicant's argument fails to identify where in the specification discloses that a subrange includes non-contiguous addresses (emphasis added). The specification merely discloses that the each subrange is materialized in a unique physical memory but the specification does not disclose that the subrange contains a non-contiguous address range within itself. Thus, the examiner suggests the applicant to delete the term "non-contiguous" from the claim limitation.

Arguments Concerning Prior Art Rejections

Further, the applicant argues that the cited prior arts fail to teach “replacing the single flash memory device having the contiguous range of logical memory addresses with the plurality of flash memory devices". However, as apparent in the corresponding claim rejection above, Daberko teaches a single flash memory device and Borkenhagen teaches a plurality of flash memory devices that can be used as on logical memory device. Thus, combining the two references results in replacing a single flash memory device with a plurality of flash memory devices.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

A. Claims No Longer in the Application

Claims 15 and 18 are cancelled.

B. Claims Rejected in the Application

Claims 1-14, 16, 17 and 19-20 have received a second action on the merits and are subject of a second action final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

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/Jae U Yu/

Examiner, Art Unit 2185

10/19/2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185